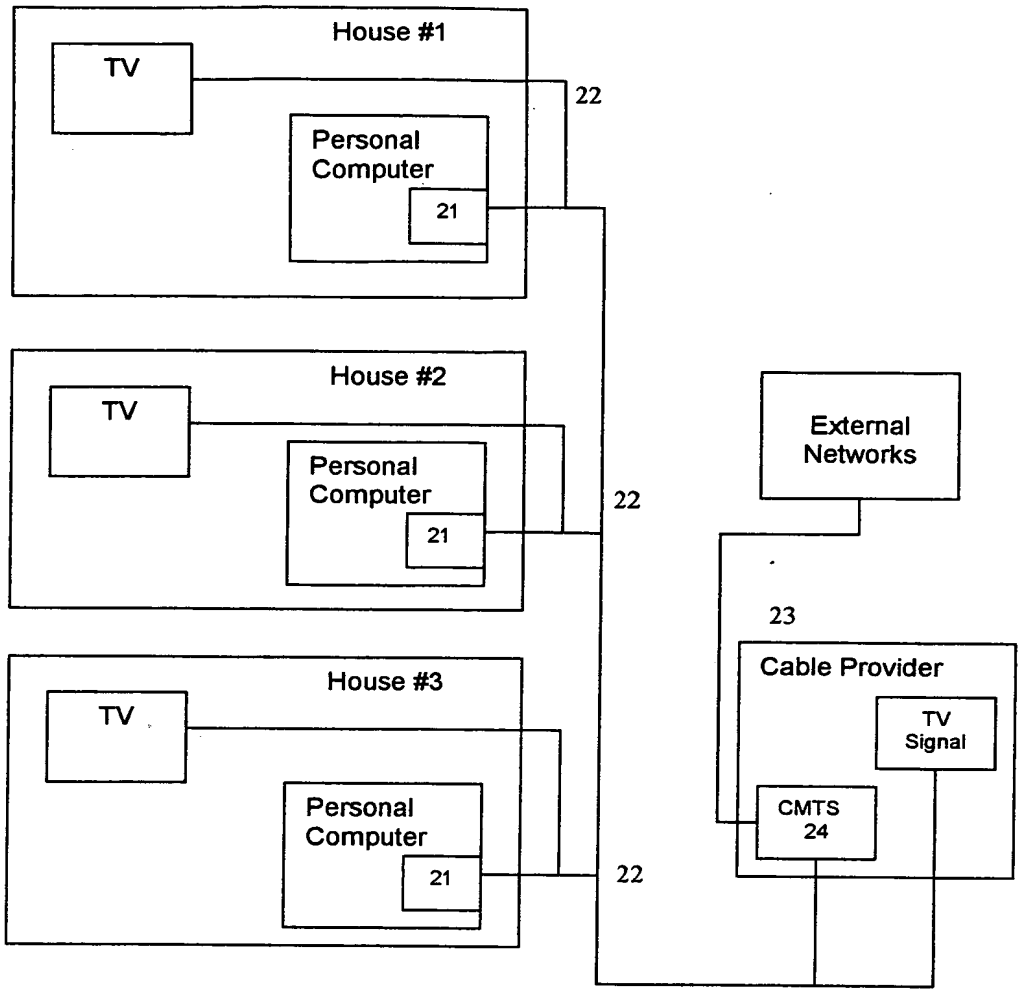

House #1
TV
Personal Computer
21
22
House #2
TV
Personal Computer
21
22
House #3
TV
Personal Computer
21
22
External Networks
23
Cable Provider
TV Signal
CMTS 24

Figure 1

FIGURE 2

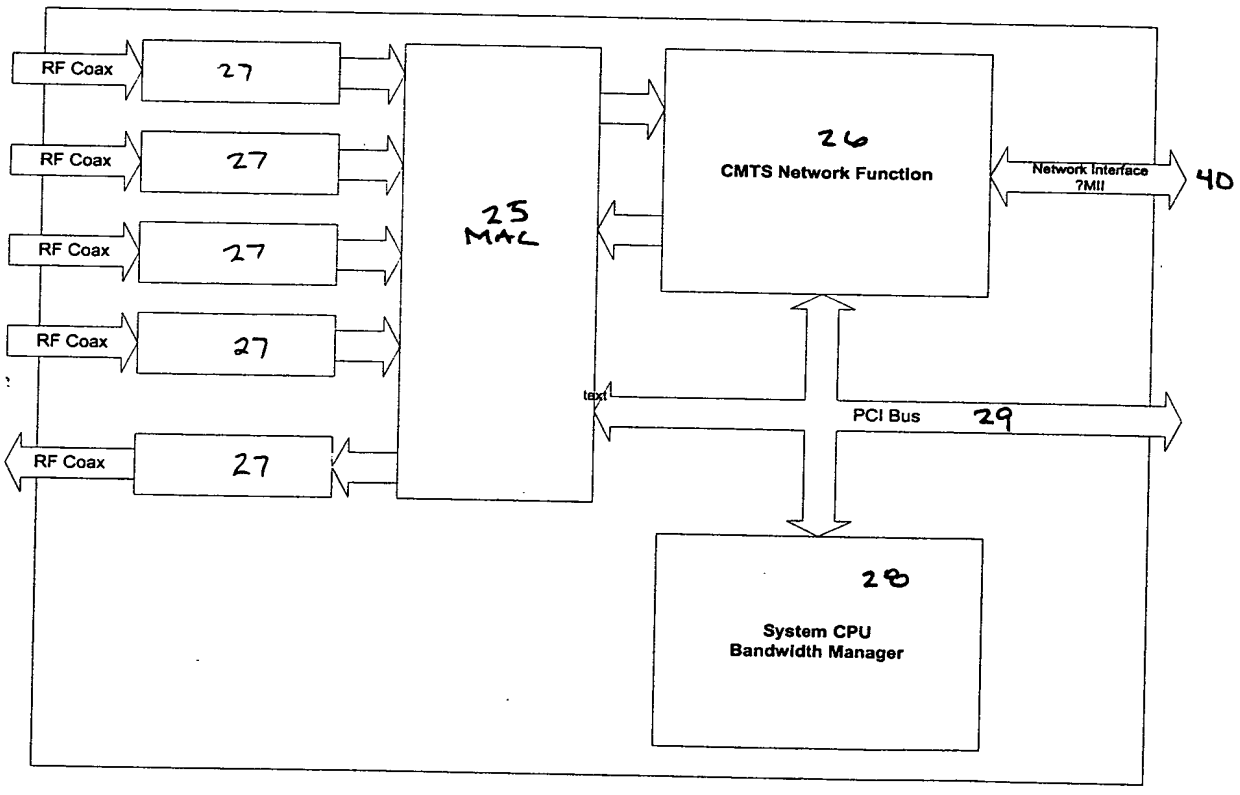
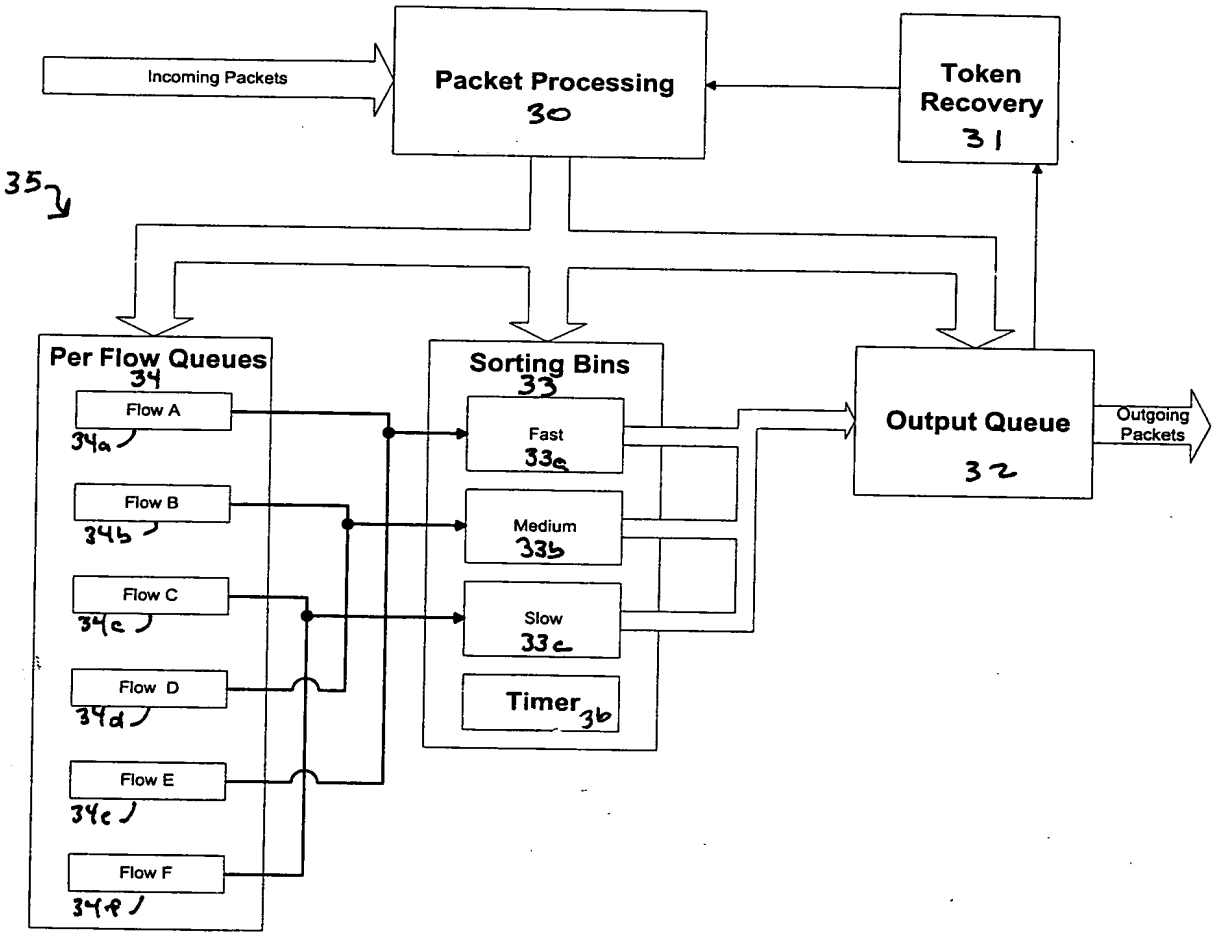

RF Coax
27
RF Coax
27
RF Coax
27
RF Coax
27
RF Coax
27
25
MAC
26
CMTS Network Function
Network Interface
7MII
40
text
PCI Bus
29
28
System CPU
Bandwidth Manager

FIGURE 3


Incoming Packets
Packet Processing
30
Token Recovery
31
35
Per Flow Queues
34
Flow A
34a
Flow B
34b
Flow C
34c
Flow D
34d
Flow E
34e
Flow F
34f
Sorting Bins
33
Fast
33a
Medium
33b
Slow
33c
Timer
36
Output Queue
32
Outgoing Packets

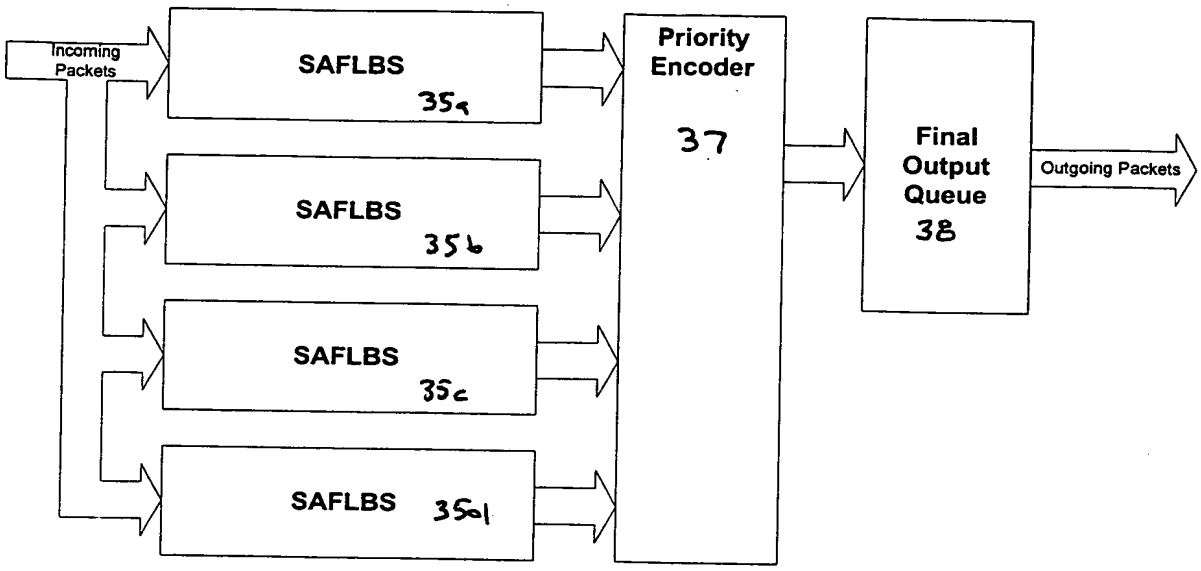

Incoming Packets
SAFLBS
35a
SAFLBS
35b
SAFLBS
35c
SAFLBS
35d
Priority Encoder
37
Final Output Queue
38
Outgoing Packets

FIGURE 4

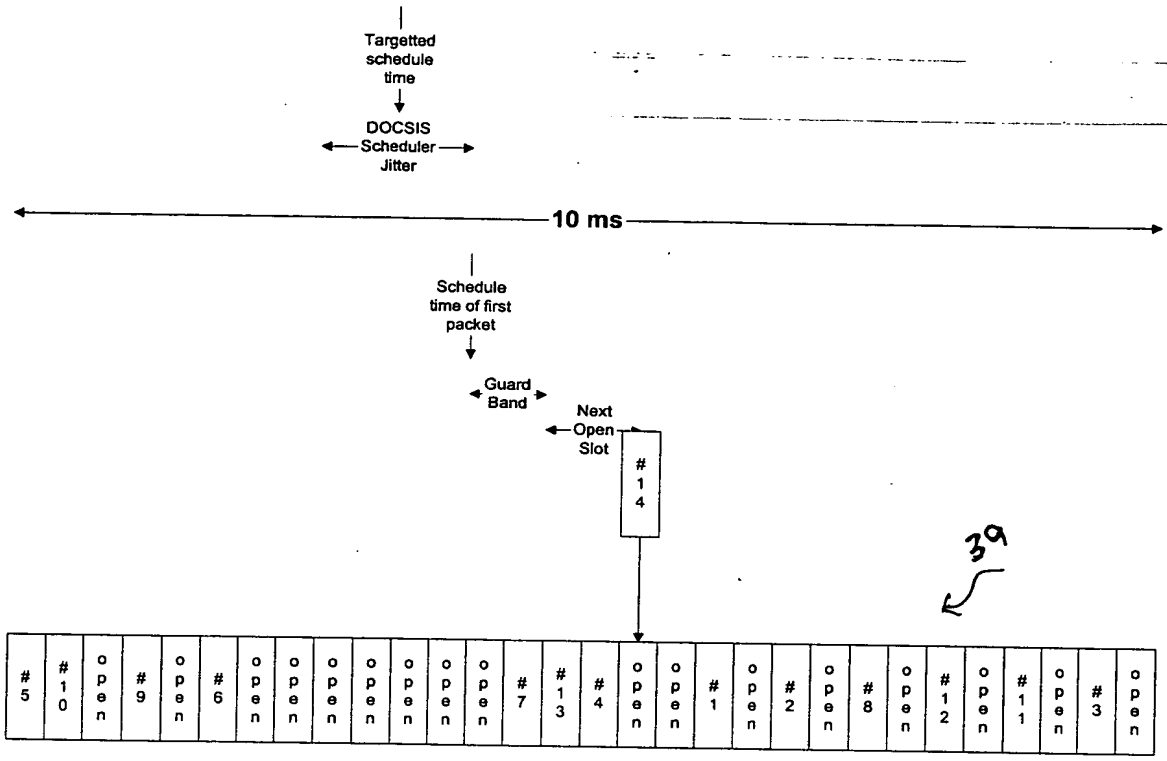

Targetted schedule time
DOCSIS Scheduler Jitter
10 ms
Schedule time of first packet
Guard Band
Next Open Slot
#14
39
#5
#10
open
#9
open
#6
open
open
open
open
open
open
open
#7
#13
#4
open
open
#1
open
#2
open
#8
open
#12
open
#11
open
#3
open

FIGURE 5

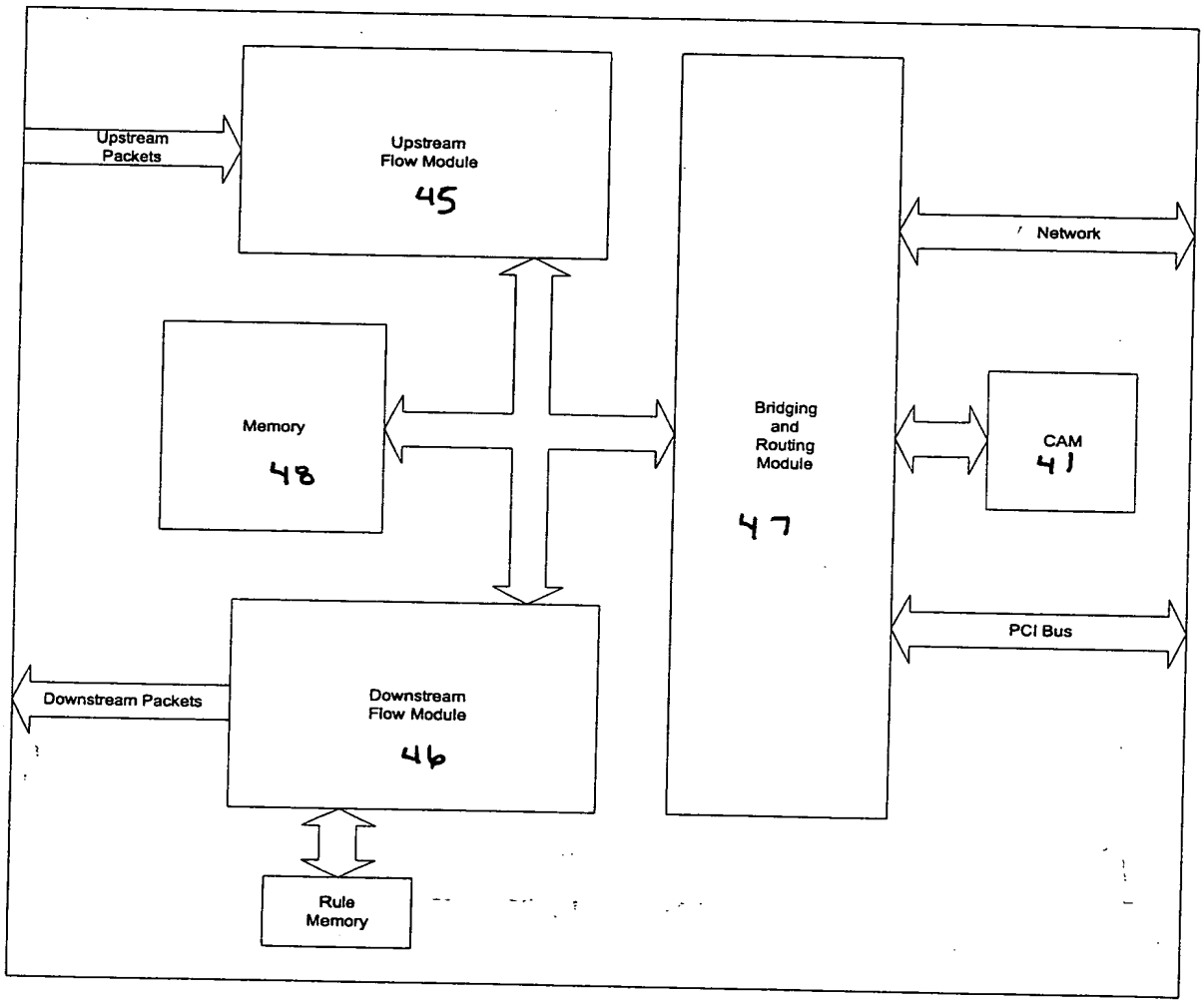

Upstream Packets
Upstream Flow Module
45
Network
Memory
48
Bridging and Routing Module
47
CAM
41
PCI Bus
Downstream Packets
Downstream Flow Module
46
Rule Memory

FIGURE 6

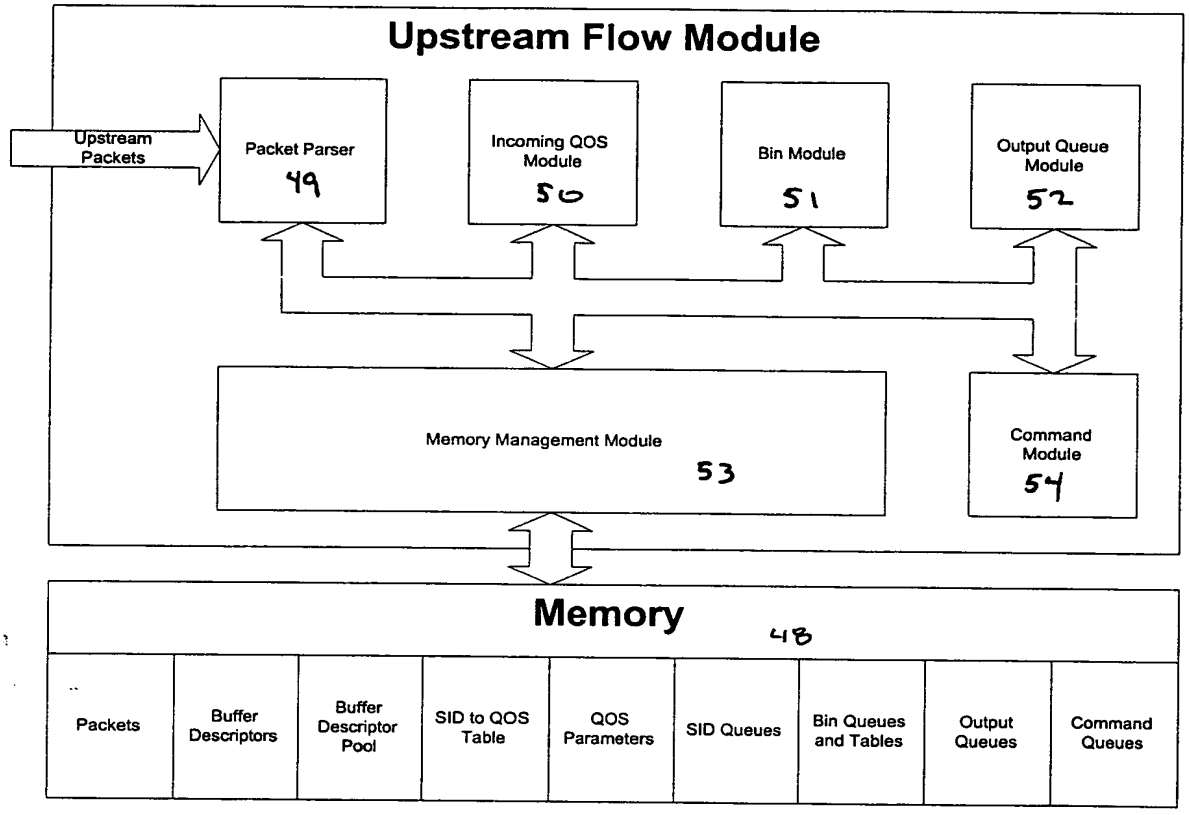
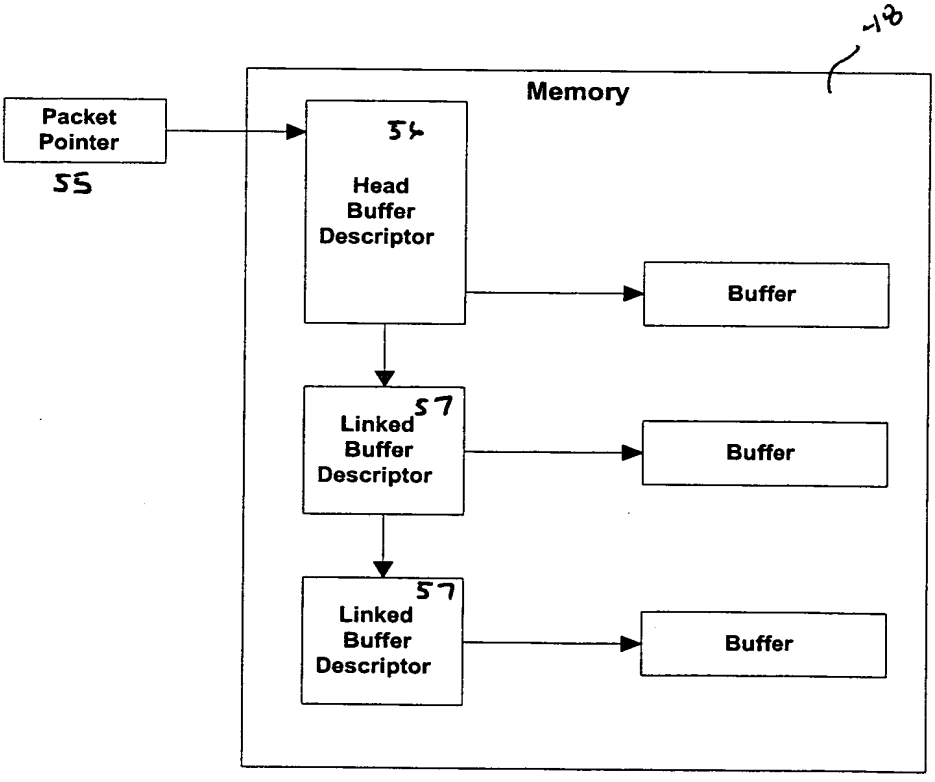

Upstream Flow Module
Upstream Packets
Packet Parser
49
Incoming QOS Module
50
Bin Module
51
Output Queue Module
52
Memory Management Module
53
Command Module
54
Memory
48
Packets
Buffer Descriptors
Buffer Descriptor Pool
SID to QOS Table
QOS Parameters
SID Queues
Bin Queues and Tables
Output Queues
Command Queues

FIGURE 7

FIGURE 8


18
Memory
Packet Pointer
55
54
Head Buffer Descriptor
Buffer
Linked Buffer Descriptor
57
Buffer
Linked Buffer Descriptor
57
Buffer

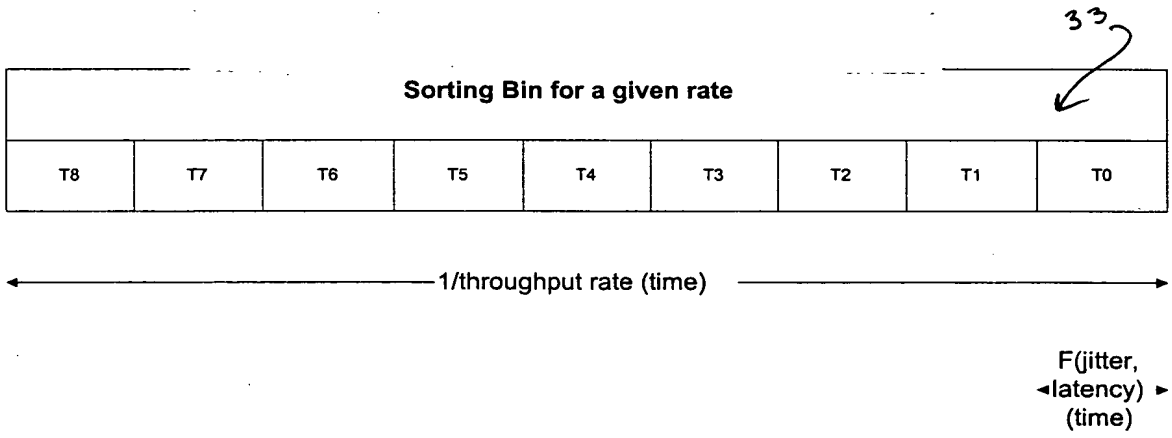

33
Sorting Bin for a given rate
T8
T7
T6
T5
T4
T3
T2
T1
T0
1/throughput rate (time)
F(jitter, latency) (time)

FIGURE 9

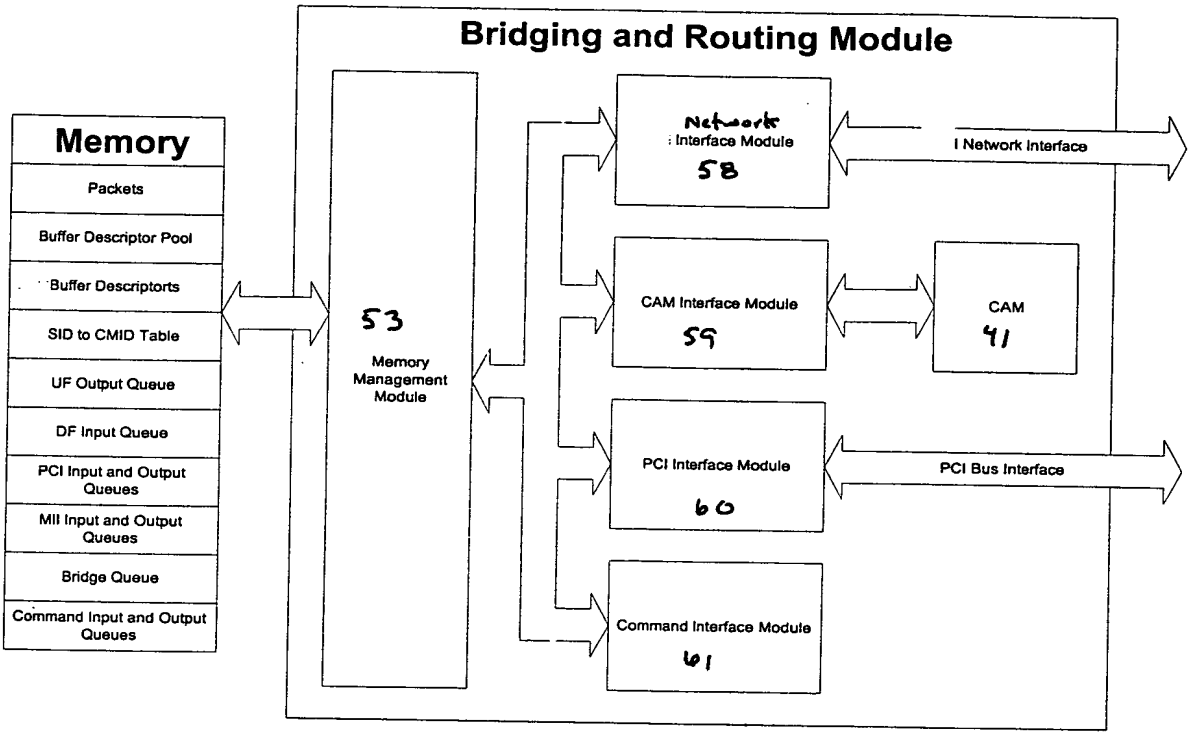

Bridging and Routing Module
Memory
Packets
Buffer Descriptor Pool
Buffer Descriptorts
SID to CMID Table
UF Output Queue
DF Input Queue
PCI Input and Output Queues
MII Input and Output Queues
Bridge Queue
Command Input and Output Queues
53
Memory Management Module
Network Interface Module
58
I Network Interface
CAM Interface Module
59
CAM
41
PCI Interface Module
60
PCI Bus Interface
Command Interface Module
61

FIGURE 10

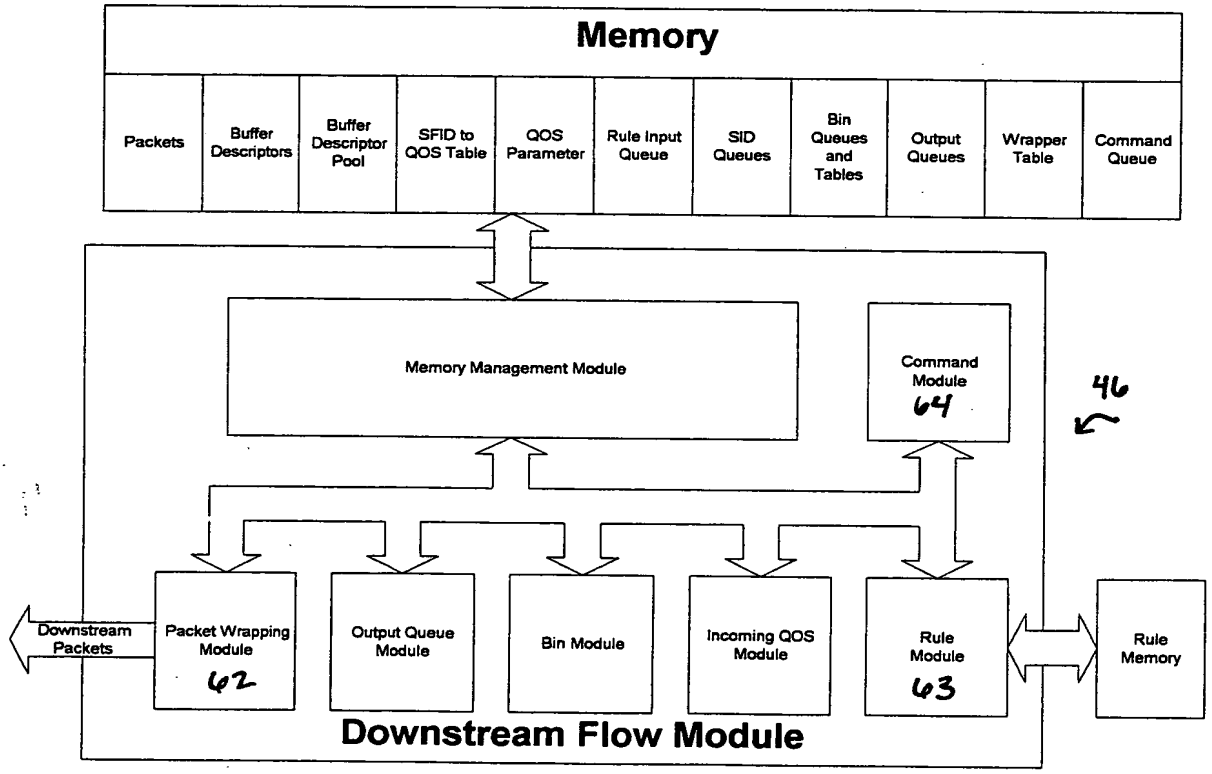

Memory
Packets
Buffer Descriptors
Buffer Descriptor Pool
SFID to QOS Table
QOS Parameter
Rule Input Queue
SID Queues
Bin Queues and Tables
Output Queues
Wrapper Table
Command Queue
Memory Management Module
Command Module
64
46
Downstream Packets
Packet Wrapping Module
62
Output Queue Module
Bin Module
Incoming QOS Module
Rule Module
63
Rule Memory
Downstream Flow Module

FIGURE 11